SALEAGLE®4D20 FPGA

Datasheet

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Content

1 Introduction

1.1 SALEAGLE®4 (hereafter refers to EG4) D20 Features

- **Flexible Architecture**
  - 19,600 LUTs
- **Low Power**
  - Advanced 55nm low power consumption technology
  - Static power consumption lower to 5mA
- **Various on-chip RAM space**
  - Embedded 9Kbits block RAM x64, Embedded 32Kbits block RAM x16
  - 128Mb DDR SDRAM memory space
  - Up to 156.8Kb distributed RAM
- **Programmable Logic Blocks (PLBs)**
  - Optimized LUT4/LUT5 combinatorial design
  - Dual-port distributed memory
  - Arithmetic function
  - Fast carry chain logic
- **Embedded Multiplier**
  - 29 18 x 18 multipliers, support 9 x 9 mode
- **Source Synchronous Input/ Output Interface**
  - Input/ Output units contain DDR register
  - Generic DDRx1
  - Generic DDRx2
  - **High-performance, flexible Input/ Output Buffer**
  - Hot socketing
  - Programmable pull-up/pull-down
  - On-chip 100Ω differential resistor
- **Clock Resource**
  - 16 global clocks
  - Four PLLs for frequency synthesis
  - Five clocks output
  - Division factor from 1 to 128
  - Five clocks output for cascading
  - Dynamic phase selection
- **Embedded Hard IP**
  - ADC
    - 12-Bit SAR
    - Maximum up to eight analog input
    - 1MHz Sampling rate (MSPS)
  - Integrate voltage monitor module
  - Internal ring oscillator

- **Configuration Mode**
  - Master SPI (MSPI)
  - Slave Serial (SS)
  - Master Parallel x8 (MP)
  - Slave Parallel x8 (SP)
  - JTAG mode (IEEE-1532)
  - Dual boot and multi boot
- **BSCAN**
  - Compatible with IEE-1149.1
- **Package**
  - QFP

Table 1-1 EG4D20 Device Selection Guide

General feature	EG4D20EG176	EG4D20EG176B
Number of FFs	19,600	19,600
Number of LUTS	19,600	19,600
Number of Dis-Ram bits	156,800	156,800
Number of ERAM (9k)	64	64
Number of ERAM (32k)	16	16
Total EBR Kbits	1,088	1,088
Number of M18x18	29	29
PLL	4	4
Low-skew GCLK	16	16
EM SDRAM	8Mx16bits	8Mx16bits
User IO Banks	8	8
Maximum user IOs	135	135

Table 1-2 EG4D20 FPGA Package

Packages	EG4D20EG176	EG4D20EG176B
QFP (20x20, 0.4mm pitch)	135/24	135/24

Note:

1. (135/24) available IO number / available LVDS pairs number

2. The calculation of "Number of Dis-Ram" is: the number provided in the software x1024, take the integral.

1.2 Introduction to EG4D20

Built on the reliable low power-consumption and programmable FPGA—EG4X20, EG4D20 FPGA integrate with one 8M x 16bits SDRAM by using the advanced 3D SIP technology. EG4D20 possess the smaller-size, easy-processing device package with larger embedded memory so that it is ideally fit for the applications like large-scale, high-speed data sampling, transmission and switching.

Special features

- Multiple devices, large-scale embedded memory
  - Embedded 128Mb DDR SDRAM memory space, 16-bit data bus line width with maximum working frequency of 200Mhz and maximum read/write bandwidth up to 800MB/S
  - Embedded 64 ERAM9K random read/write RAM that can be configured as true dual-port, simple dual-port, single-ended RAM and FIFO working mode. Bit wide can be configured as 512x18, 1Kx9, 2Kx4, 4Kx2, 8Kx1 with maximum frequency of 250Mhz.
  - Embedded 16 32Kb RAM that can be configured as single-port RAM, dual-port RAM and can be independently configured as 2Kx16 or 4Kx8
- Smaller package with more IO that is beneficial for PCB routing and pin layout
  - QFP176 Package, EPAD connect to ground with maximum up to 135 user I/Os
  - Support True LVDS with maximum frequency of 800Mbps
  - QFP176 Package specification: 20mm x 20mm, 0.4mm fine pitch
  - optimized pin layout, only two layers of PCB can enable all devices I/Os
  - Support easy and low-cost SPI FLASH configuration; after power-on configuration, FLASH can be used by users
- Integrate multiple dedicated IP
  - Integrate 12BIT SAR ADC, sampling rate up to 1MHz and support up to eight input channels multiplexing

- Integrate voltage monitor module, you can modify monitoring which BANK voltage
- Integrate internal ring oscillator

2 EG4D20 Architecture

Same as EG4X20, for more details, please refer to EG4 datasheet

3 EG4D20 AC/DC Characteristics

Same as EG4X20, for more details, please refer to EG4 datasheet

4 EG4D20 Internal SDRAM

EG4D20 embed one 8M X16bit DDR SDRAM (W9412G6KH) with the maximum working frequency of 200Mhz and the maximum read/write bandwidth up to 800MB/s. EG4D20EG176B internal SRAM EM6A9160GDD. SDRAM is deeply integrated with FPGA through the software. You only have to instantiate in IP generate or instantiate the following IP module at top when you need SDRAM. The IP prototype as shown in the following.

```
EG_PHY_SDRAM_128  U_EG_PHY_SDRAM_128(

.clk(SD_CLK),        // SDRAM differential clock positive 1bit width

.clk_n(SD_CLK_N),    // SDRAM differential clock negative 1bit width

.ras_n(SD_RAS_N),    // SDRAM row address strobe 1bit width

.cas_n(SD_CAN_N),   //SDRAM column address strobe 1bit width

.we_n(SD_WE_N),   //SDRAM write enable 1bit width

.cs_n(SD_CS_N),     //SDRAM chipselect 1bit width

.addr(SD_SA),        //SDRAM address 11bits width

.ba(SD_BA),         // SDRAM BANK address 2bits width

.dq(SD_DQ),         //SDRAM data 16 bits width

.ldqs(SD_LDQS),     // SDRAM low bit data strobe signal 1bit width

.udqs(SD_UDQS),    // SDRAM high bit data strobe signal 1bit width

.ldm(SD_LDM),      // SDRAM low bit data mask signal 1bit width
```

```
.udm(SD_UDM),     // SDRAM high bit data mask signal 1bit width
.cke(SD_CKE)      // SDRAM clock enable 1bit width
);
```

Table 4-1 SDRAM Pin Distribution

SDRAM Pin	SDRAM Pin Description	Connection	Direction
DQ0	Data pin 0	Connect to IP	Bi-directional
DQ1	Data pin 1	Connect to IP	Bi-directional
DQ2	Data pin 2	Connect to IP	Bi-directional
DQ3	Data pin 3	Connect to IP	Bi-directional
DQ4	Data pin 4	Connect to IP	Bi-directional
DQ5	Data pin 5	Connect to IP	Bi-directional
DQ6	Data pin 6	Connect to IP	Bi-directional
DQ7	Data pin 7	Connect to IP	Bi-directional
DQ8	Data pin 8	Connect to IP	Bi-directional
DQ9	Data pin 9	Connect to IP	Bi-directional
DQ10	Data pin 10	Connect to IP	Bi-directional
DQ11	Data pin 11	Connect to IP	Bi-directional
DQ12	Data pin 12	Connect to IP	Bi-directional
DQ13	Data pin 13	Connect to IP	Bi-directional
DQ14	Data pin 14	Connect to IP	Bi-directional
DQ15	Data pin 15	Connect to IP	Bi-directional
ADDR0	Address pin 0	Connect to IP	Output
ADDR1	Address pin 1	Connect to IP	Output
ADDR2	Address pin 2	Connect to IP	Output
ADDR3	Address pin 3	Connect to IP	Output
ADDR4	Address pin 4	Connect to IP	Output
ADDR5	Address pin 5	Connect to IP	Output
ADDR6	Address pin 6	Connect to IP	Output
ADDR7	Address pin 7	Connect to IP	Output
ADDR8	Address pin 8	Connect to IP	Output

SDRAM Pin	SDRAM Pin Description	Connection	Direction
ADDR9	Address pin 9	Connect to IP	Output
ADDR10	Address pin 10	Connect to IP	Output
ADDR11	Address pin 11	Connect to IP	Output
BA0	BANK Address pin 0	Connect to IP	Output
BA1	BANK Address pin 1	Connect to IP	Output
WE_N	Write enable	Connect to IP	Output
RAS_N	Row address strobe	Connect to IP	Output
CAS_N	Column address strobe	Connect to IP	Output
CLK	Chip clock positive	Connect to IP	Output
CLK_N	Chip clock negative	Connect to IP	Output
LDQS	Low bit data strobe	Connect to IP	Bi-directional
UDQS	High bit data strobe	Connect to IP	Bi-directional
LDM	low bit data mask	Connect to IP	Output
UDM	high bit data mask	Connect to IP	Output
CKE	clock enable	Connect to IP	Output
CS_N	Chipselect	Connect to IP	Output

5 Pin and Package

5.1 Pin Definition

Table 5-1 Pin Definition Rule

Pin	Direction	Description
Power GND Pin		
NC	—	No connection
GND	—	Power Ground
GND_EPAD	—	Chip GND PAD
VCC	—	Supply voltage for core
VCCIOx	—	Supply voltage for I/O BANK
VCCAUX	—	Auxiliary voltage
VCC_PLLX	—	PLL voltage
GND_PLLx	—	PLL Ground
JTAG Dedicated PIN		
TCK	Input	TCK input boundary scan clock
TDI	Input	Boundary scan data input
TDO	Output	Boundary scan data output
TMS	Input	Boundary scan mode select
Configuration Dedicated Pin		
CSI_B	Input	Parallel download mode chipselect signal, low active
MSEL[2:0]	Input	Download mode select
PROGRAMN_B	Input	Global reset input, low active
CCLK	I/O	—
DONE	I/O	Dedicated configuration pin, output high after configuration, source open-drain
INITB	I/O	Dedicated configuration status pin, output high indicates FPGA configuration ready, source open-drain

CSO_B	I/O	FLASH chipselect
HSWAPEN	I/O	I/O loading state control pin

5.2 EG4D20EG176/B FPGA Pin List

No.	BANK [1]	Name	Description	Min System requirement
1	1	VCC	Internal voltage	Yes
2	1	IO_L1N_1	User I/O	
3	1	IO_L1P_1	User I/O	
4	1	IO_L2N_1	User I/O	
5	1	DDR_VREF	DDR ref voltage, 1/2 VDD	Yes
6	1	IO_L2P_1	User I/O	
7	1	VCCIO1	2.5-3.3V BANK1 IO voltage	Yes
8	1	IO_L1_1	User I/O	
9	1	GND	Chip Ground	Yes
10	1	IO_L3P_1,DONE	Configuration done/User I/O	
11	1	IO_L3N_1	User I/O	
12	1	VCCIO1	2.5-3.3V BANK1 IO voltage	Yes
13	1	GND	Chip Ground	Yes
14	1	IO_L4P_1	User I/O	
15	1	IO_L4N_1	User I/O	
16	1	IO_L5N_1	User I/O	
17	1	IO_L5P_1	User I/O	
18	1	VCCIO1	2.5-3.3V BANK1 IO voltage	Yes
19	1	IO_L2_1,GCLKIOL_3	User I/O	
20	1	VCC	Internal voltage	Yes

No.	BANK [1]	Name	Description	Min System requirement
21	1	GND	Chip Ground	Yes
22	2	IO_L1P_2,GCLKIOL_5	User I/O	
23	2	IO_L1N_2,GCLKIOL_4	User I/O	
24	2	VCCIO2	2.5-3.3V BANK2 IO voltage	Yes
25	2	IO_L1_2,GCLKIOL_6	User I/O	
26	2	IO_L2P_2	User I/O	
27	2	IO_L2N_2	User I/O	
28	2	IO_L3P_2	User I/O	
29	2	IO_L3N_2	User I/O	
30	2	IO_L4N_2	User I/O	
31	2	IO_L4P_2	User I/O	
32	2	IO_L2_2	User I/O	
33	2	GND	Chip ground	Yes
34	2	VCCIO2	2.5-3.3V BANK2 IO voltage	Yes
35	2	IO_L3_2	User I/O	
36	2	IO_L5N_2	User I/O	
37	2	IO_L5P_2	User I/O	
38	2	GND	Chip ground	Yes
39	2	IO_L4_2	User I/O	
40	2	VCCIO2	2.5-3.3V BANK2 IO voltage	Yes
41	2	IO_L6N_2	User I/O	
42	2	IO_L6P_2	User I/O	
43	2	IO_L5_2,JTAG_TDO	JTAG/User I/O	Yes

No.	BANK [1]	Name	Description	Min System requirement
44	2	IO_L6_2,JTAG_TMS	JTAG/User I/O	Yes
45	-	VCCAUX	Auxiliary voltage	Yes
46	3	IO_B1_3,JTAG_TDI	JTAG/User I/O	Yes
47	3	IO_B2_3,JTAG_TCK	JTAG/User I/O	Yes
48	3	VCC	Internal voltage	Yes
49	3	IO_BE1N_3	User I/O	
50	3	IO_BE1P_3	User I/O	
51	3	IO_BE2N_3	User I/O	
52	3	IO_BE2P_3	User I/O	
53	3	IO_BE3P_3	User I/O	
54	3	IO_BE3N_3	User I/O	
55	3	IO_B3_3	User I/O	
56	3	IO_B4_3	User I/O	
57	3	IO_BE4N_3	User I/O	
58	3	IO_BE4P_3	User I/O	
59	3	VCCIO3	BANK3 IO voltage	Yes
60	3	IO_BE5N_3,GCLKIOB_4	User I/O	
61	3	IO_BE5P_3,GCLKIOB_5	User I/O	
62	4	IO_BE1N_4,GCLKIOB_2	User I/O	
63	4	IO_BE1P_4,GCLKIOB_3	User I/O	
64	4	IO_BE10N_4	User I/O	
65	4	VCC	Internal voltage	Yes
66	4	IO_BE10P_4	User I/O	

No.	BANK [1]	Name	Description	Min System requirement
67	4	VCCIO4	BANK4 IO power	Yes
68	4	IO_BE2P_4	User I/O	
69	4	IO_BE2N_4	User I/O	
70	4	IO_BE3P_4	User I/O	
71	4	IO_BE3N_4	User I/O	
72	4	IO_B3_4	User I/O	
73	4	IO_BE4P_4	User I/O	
74	4	IO_BE4N_4	User I/O	
75	4	IO_BE5N_4	User I/O	
76	4	IO_BE5P_4	User I/O	
77	4	IO_BE6N_4	User I/O	
78	4	IO_BE6P_4	User I/O	
79	4	IO_BE7P_4	User I/O	
80	4	VCCIO4	BANK4 IO voltage	Yes
81	4	IO_BE7N_4	User I/O	
82	4	IO_BE8N_4	User I/O	
83	4	IO_BE8P_4	User I/O	
84	4	IO_BE9N_4	User I/O	
85	4	VCC	Internal voltage	Yes
86	4	IO_BE9P_4	User I/O	
87	4	VCCAUX	Auxiliary voltage	Yes
88	4	IO_B4_4,HSWAPEN	IO Status selection during program loading	

No.	BANK [1]	Name	Description	Min System requirement
89	5	IO_R1N_5	User I/O	
90	5	IO_R1P_5	User I/O	
91	5	IO_R1_5	User I/O	
92	5	VCC	Core voltage	Yes
93	5	IO_R2P_5	User I/O	
94	5	IO_R2N_5	User I/O	
95	5	IO_R3N_5	User I/O	
96	5	VCCIO5	2.5-3.3V BANK5 voltage	Yes
97	5	IO_R3P_5	User I/O	
98	5	IO_R4P_5	User I/O	
99	5	IO_R4N_5	User I/O	
100	5	IO_R5P_5	User I/O	
101	5	IO_R5N_5	User I/O	
102	5	IO_R6N_5	User I/O	
103	5	IO_R6P_5	User I/O	
104	5	IO_R2_5	User I/O	
105	5	VCCIO5	2.5-3.3V BANK5 voltage	Yes
106	5	IO_R7P_5	User I/O	
107	5	IO_R7N_5	User I/O	
108	5	VCCIO5	2.5-3.3V BANK5 voltage	Yes
109	5	IO_R3_5	User I/O	
110	5	IO_R8N_5	User I/O	
111	5	IO_R8P_5	User I/O	

No.	BANK [1]	Name	Description	Min System requirement
112	5	IO_R4_5	User I/O	
113	6	VCC	Core voltage	Yes
114	6	IO_R1_6, GCLKIOR_2	User I/O	
115	6	IO_R2_6, GCLKIOR_4	User I/O	
116	6	GND	Chip ground	Yes
117	6	VCCIO6	2.5-3.3V BANK6 voltage	Yes
118	6	IO_R3_6	User I/O	
119	6	IO_R4_6	User I/O	
120	6	VCCIO6	2.5-3.3V BANK6 IO voltage	Yes
121	6	IO_R1P_6	User I/O	
122	6	IO_R1N_6	User I/O	
123	6	IO_R2N_6	User I/O	
124	6	IO_R2P_6	User I/O	
125	6	VCCIO6	2.5-3.3V BANK6 IO voltage	Yes
126	6	IO_R3P_6	User I/O	
127	6	IO_R3N_6	User I/O	
128	6	VCC	Core voltage	Yes
129	6	IO_R4N_6	User I/O	
130	6	IO_R4P_6	User I/O	
131	6	IO_R5P_6	User I/O	
132	6	IO_R5N_6	User I/O	
133	7	IO_TE1P_7	User I/O	
134	7	IO_TE1N_7, PROGRAM_B	User I/O/ chip	Yes

No.	BANK [1]	Name	Description	Min System requirement
			reset	
135	7	VCCAUX	Auxiliary voltage	Yes
136	7	IO_TE2P_7	User I/O	
137	7	VCC	Core voltage	Yes
138	7	IO_TE2N_7	User I/O	
139	7	IO_TE3P_7, INITB	User I/O	
140	7	IO_TE3N_7, CSO_B	FLASH chipselect /User I/O	
141	7	IO_TE11N_7	User I/O	
142	7	VCCIO7	BANK7 IO voltage	Yes
143	7	IO_TE11P_7	User I/O	
144	7	IO_TE4P_7	User I/O	
145	7	IO_TE4N_7	User I/O	
146	7	IO_TE5P_7, D3	User I/O	
147	7	IO_TE5N_7, D4	User I/O	
148	7	IO_T3_7	User I/O	
149	7	IO_TE6P_7	User I/O	
150	7	IO_TE6N_7	User I/O	
151	7	IO_T4_7	User I/O	
152	7	IO_TE7P_7, D7	User I/O	
153	7	IO_TE7N_7	User I/O	
154	7	VCCIO7	BANK7 IO voltage	Yes
155	7	IO_TE8N_7, D6	User I/O	
156	7	IO_TE8P_7, D5	User I/O	

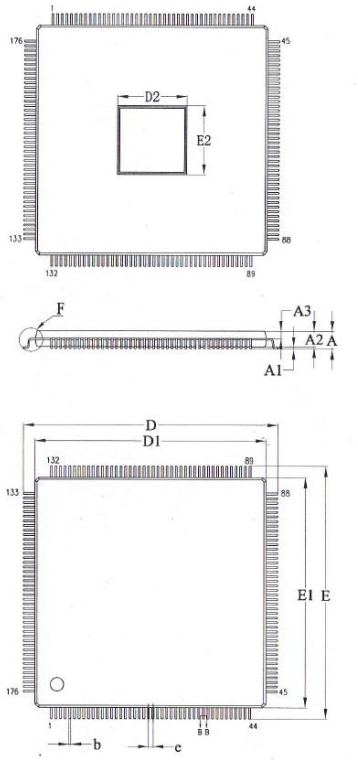
No.	BANK [1]	Name	Description	Min System requirement
157	7	IO_T5_7, GCLKIOT_7	User I/O	
158	7	IO_TE9N_7, GCLKIOT_4	User I/O	
159	7	IO_TE9P_7, GCLKIOT_5	User I/O	
160	7	VCCIO7	BANK7 IO voltage	Yes
161	7	IO_T6_7, GCLKIOT_0	User I/O	
162	7	IO_TE10P_7, GCLKIOT_3	User I/O	
163	7	IO_TE10N_7, GCLKIOT_2	User I/O	
164	8	VCC	Core voltage	Yes
165	8	IO_T1_8, DO_DIN_MISO	FLASH data output/User I/O	
166	8	IO_T2_8, MOSI, CSI_B	FLASH data input/User I/O	
167	8	VCCIO8	BANK8 IO voltage	Yes
168	8	IO_T3_8, CCLK	FLASH clock/User I/O	
169	8	IO_T4_8, M0	Mode selection/User I/O	
170	8	IO_T5_8, M1, ADC_CH_0	Configuration mode selection/ADC input	
171	8	VCCIO8	BANK8 IO voltage	Yes
172	8	IO_TE2P_8, D1, ADC_CH_5, ADC_VREF	ADC reference voltage input	Yes
173	8	IO_TE1P_8, GPLL1_CLKIN0, ADC_CH_4	ADC input/User I/O	
174	8	IO_TE2N_8, D2, ADC_CH_6	User I/O	
175	8	VCCAUX	Auxiliary	Yes

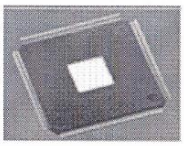
No.	BANK [1]	Name	Description	Min System requirement
			voltage	
176	8	IO_TE1N_8,GPLL1_CLKIN1,ADC_CH_7	ADC input/User I/O	
177		GND_EPAD	Chip ground PAD	Yes

Note:

1. BANK1, BANK2, BANK5 and BANK6 are connected with each other internally and should be supplied with same voltage range from 2.5V-3.3V, BANK3 IO voltage is connected with VCCAUX internally, VCCIO3 and VCCAUX must have the same voltage. It can either be 3.3V or 2.5V. other banks can support 1.2V, 1.5V, 1.8V,2.5V,3.3V IO voltage.

5.3 EG4D20EG176/B Package Specifications





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

	D2	E2
236*236	6.00REF	6.00REF
290*290	7.00REF	7.00REF

6 Ordering Information

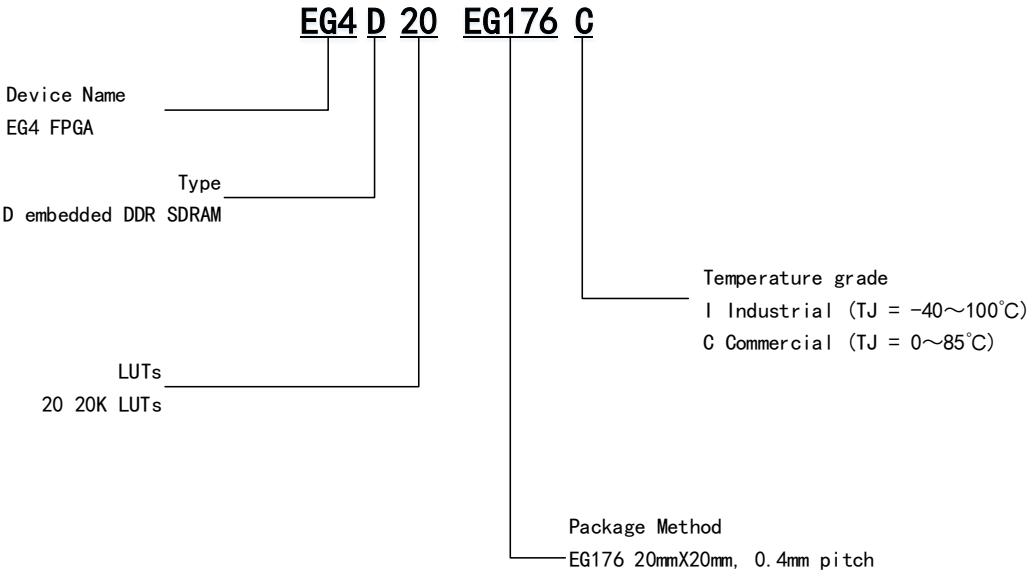
Table 6-1 Device Abbreviation

Device Name	Type	LUT	Package Type	Temperature grade
EG4	D	20	EG176	I

- Device family
  - ✧ EAGLE family
- Type
  - ✧ D Embedded DDR SDRAM
- LUT
  - ✧ 20 20K LUTs
- Package Type: <type><#>
  - ✧ EG QFP
  - ✧ # pin number (176 refers to 176 pins)
- Temperature grade
  - ✧ C Commercial (TJ = 0 - 85 ℃)
  - ✧ I Industrial (TJ = -40 - 100 ℃)

Note:

1. The symbol of "C" and "C7" on the inner box are the same type of symbol.



Note:

1. EG4D20EG176B package and pin same as EG4D20EG176, the only difference lies in different SDRAM model that integrated in EG4D20EG176; EG4D20EG176 internal SDRAM model is W9412G6KH, EG4D20EG176B internal SDRAM model is EM6A9160GDD.

Revision History

Date	Version	Change
2024/07/20	1.3.4	1. Delete parameter specification on chapter 1.1 2. Delete Master Serial PROM(MS) on chapter 1.1 3. Delete Total Configuration SRAM (bits) on Table 1-1 4. Add note after Table 1-2 5. Update Total EBR Kbits unit on Table 1-1 6. Update Table 1-2 differential pairs number 7. Update Table 5-1 8. Update chapter 5.2 pinlist 9. Update the note after chapter 6 10. Unify package name, modify "eTQFP", "eLQFP" into "QFP".
2022/1/4	1.3.3	Update package description

Disclaimer